Please amend the present application as follows:

Specification

The following is a marked-up version of the specification with the language that is underlined ("___") being added and the language that contains strikethrough ("~~___~~") being deleted:

Page 7, lines 15 through 26.

A phase splitter 600 is shown in a closed loop system for phase correction in Fig. 6. The phase splitter 600 is similar to the phase splitter 400, as will be seen. In this embodiment, the output of a local oscillator 601 is connected to input terminals 417, 419 and variable resistors 603, 605 are connected across the terminals 428, 426 and 422, ~~426~~ 424, respectively.

In this embodiment, the resistors 603, 605 are MOS transistor devices. The drain and source of the transistor 603 are connected across terminals 428, 426, and the drain and source of the transistor 605 are connected across terminals 422, ~~426~~ 424.

The output terminals 428, 426 represent the I quadrature, and are processed through a mixer 602 and baseband circuitry 604, to an output 606. Similarly, the output terminals 422, ~~426~~ 424 represent the Q quadrature signals, and they are processed through a mixer 608 and baseband circuitry 610 to an output 612.

Page 10, lines 3 through 23.

An analog-to-digital converter (ADC) 1002, a latch 1004, and a digital-to-analog converter (DAC) 1006 could be used instead of the integrator 616, differential amplifier ~~418~~

618 and capacitor 700 in Fig. 7, if desired, as seen in Fig. 10. The analog to digital converter 1002 is connected to the phase detector 614, and the latch 1004 stores the digital value determined by the ADC 1002. The analog output of the DAC 1006 is fed to the variable resistors 603, 605 in Fig. 7. Generally, digital storage is well suited for power on and reset processes in Time Division Multiple Access (TDMA) systems.

In operation, an RF test signal from the source 514 (Fig. 5) is mixed with the local oscillator signal 500 in mixers 506, 508, to produce a baseband or intermediate frequency (IF) signal having I and Q components 510, 512. The phase of the I and Q components is detected in the phase detector 515, and if the phase difference is not 90□, the error signal is stored in memory 516, which adjusts the variable resistors 504 to adjust their effective resistance. In Figs. 6 and 7, for example, the transistors 603, 605 are biased in their linear or triode range, so that even small changes at their gates produce effective resistance changes across their drains and sources, slightly adjusting the phases of the I and Q signals from the local oscillator 500. After phase adjustment, a ~~on~~ RF carrier signal encoded with a voice communication, data communication or the like is mixed with the phase adjusted local oscillator signals and decoded.